Capacitor dynamic compensation sampling voltage

What does V mean on a sampling capacitor?

During the holding period, the voltage change, ? V, on the sampling capacitor Cs caused by the leakage current Ileakage from the MOS sampling switch is given as ? V = Ileakage / (2 FsCs), where Fs is the sampling rate of the ADC. The least-significant-bit (LSB) of the N -bit ADC is defined as LSB = Vref /2 N in which Vref is the reference voltage.

What is a dynamic switch leakage compensation circuit?

A S/H circuitwith dynamic switch leakage compensation is presented. The proposed leakage current compensation circuit generates switch leakage replicas that track the actual leakages in the sampling switches. A bidirectional current steering circuit allows the switch leakage to be dynamically compensated with the leakage replicas.

Can a sampling capacitor droop?

The switch is not ideal, since it has a leakage path that can cause either a droop or a rise of the voltage held on the sampling capacitor, depending on the direction of the leakage. This is especially severe under harsh operating conditions, such as in the oil and gas exploration industry, where the operating temperature can be above 200°C.

What is a dynamic leakage current compensation technique?

A dynamic leakage current compensation technique is proposed for the S/H circuit. The new S/H circuit is capable of compensating the switch leakage currents regardless of whether the leakage is from the PMOS or the NMOS switch or both,and has a very small area penalty of only 0.01 mm 2 in the chosen technology.

How to reduce sampling nonlinearity in MIM capacitors?

A compensation structureis proposed to alleviate the sampling nonlinearity due to the charge injection from sampling switch,while the nonlinearity caused by the MIM capacitor's voltage coefficients is cancelled digitally with the assistance of pseudo-random signal injection.

What causes capacitor mismatch & sampling errors in Digital Domain?

The capacitor mismatch and sampling errors due to the capacitor's voltage coefficientsare calibrated in digital domain.

The grading capacitor is a conventional method to guarantee the uniform voltage distribution (VD) of double-break vacuum circuit breakers (VCBs). However, the main shield voltage ...

The proposed compensation technique is based on the schematic as shown in Figure 9 in which compensation is provided through a compensating transformer which is ...

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The voltage equation of a bus capacitor in Figure 1 can be written as: ... If the buck converter adopts single-voltage closed-loop control, the dynamic compensation of voltage can be achieved by adding only Q p,i. If the ...

by compensation capacitor C t1 and compensation resistor R t1. The pole and zero symbols marked "" 0"" represent the poles and zeros generated under heavy loads; otherwise, they refer ...

Statcom, Current sampling and voltage sampling . Current and Voltage Sampling in STATCOM. Static Synchronous Compensator (STATCOM) is a device used for ...

The bootstrap capacitor C1 charges the sampling switch M8; thus, the gate-source voltage of the sampling switch is fixed near VDD. In this state, the output voltage follows the input signal. ...

A distribution static compensator (DSTATCOM) is used for power quality improvement in the distribution system. ... a simple dynamic dc voltage regulation is proposed ...

A Dynamic Real-time Capacitor Compensated Inductive Coupling Transceiver ..., Guseong-dong, Yuseong-gu, Daejeon, 305-701, Republic of Korea E-mail: sklee@eeinfo.kaist.ac.kr Abstract A ...

This paper presents a novel modeling approach for flying capacitor dynamics in boost-type multi-level converters (FCML-boosts) controlled by Phase Shift Pulse Width ...

The fact that "reactions" are possible with power semiconductors within a network cycle increases the application area of a dynamic reactive power compensation system to include also voltage ...

A 1.5MSPS, 120 dB SFDR, ±10 V input range SAR ADC with sampling nonlinearity compensation and inherent 2-b coarse ADC for MSBs decision. Authors: Hongrui ...

However, the boosted voltage, which can be significantly reduced due to charge-sharing caused by parasitic capacitance at the gate of the sampling transistor MS, which is ...

For sample-and-hold (S/H) circuits operating at low sampling rate and high temperature, the switch leakage current is one of the major error sources. A S/H circuit with dynamic switch ...

As Figure 1a shows, the connection of the bottom plates of least significant bit (LSB) capacitors is the same as the digital output (D OUT) of LSBs of the previous cycle (n - 1) ...

In this paper an optimization on recently designed switched-capacitor dynamic- element- matching amplifier is presented. The main problem of this circuit is switch-charge injection.

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The voltage harmonics and voltage unbalance, as well as voltage drop due to the electrical faults, can damage the sensitive loads. Various voltage compensators, such as the ...

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